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2815

INTELLECTUAL PROPERTY LAW
FACSIMILE TRANSMITTAL SHEET

To:	Examiner Nguyen	**From:**	Mary Carter
Fax:	703-308-7382	**Pages:**	4 (Including Cover Sheet)
Re:	09/653,295	**Date:**	November 4, 2003

☐ **Urgent!** ☐ **For Review** ☐ **Please Comment** ☐ **Please Reply**

• **Comments:**

Enclosed is a copy of the response that was filed yesterday via regular mail. Mr. Romano would like a telephone conference with you today regarding this matter. Please contact me at (407) 371-3336 and advise me of your availability to speak with Mr. Romano today.

Mary Carter
Asst to Fred Romano

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IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Date of Deposit 11-3-03
I hereby certify that this Notice of Appeal is being deposited with the United States Postal Service "First Class Mail" on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
Mary V Carter
(Printed name of person mailing paper or fee)
(Signature of person mailing paper or fee)

Inventor(S)	Frank Hui Yifeng Yan Allen Yen	Case:	3-6-16
Serial No.	09/653.295	Group Art Unit:	2815
Filing Date	08/31/2000	Examiner:	Nguyen, Cuong

Title: Stacked Structure For Parallel Capacitors And Method of Fabrication

#19 Letter Amendment 11/24/03

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D. C. 20231

SIR:

Request For Removal of Improper Finality In Final Office Action and Response To Examiner's Rejections Set Forth Therein

I. REQUEST FOR REMOVAL OF IMPROPER FINALITY IN FINAL OFFICE ACTION

This paper is in response to the new final office action mailed August 4, 2003 in which the examiner withdrew the finality of the final rejection "in paper 10 filed on 8-26-01" apparently intending to reference the office action mailed 8-26-02. At the time of the mailing of the new final office action all of the claims were on appeal and applicants' appeal brief had been filed. Without expressly withdrawing the claims from appeal the examiner has made new art of record and has relied upon such art to present new grounds of rejection in a new final office action.

Applicants cannot understand the basis for the finality of the office action since the claims were on appeal and applicants have not amended the claims. Nonetheless the examiner states:

> "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP [sec.] 706.07(a)."

The examiner's reference to MPEP sec. 706.07(a) is entirely incorrect. In fact, the cited section states that the "second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither

necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement ..."

There have been no amendments to the claims since applicants' response to the first office action on the merits. Further, applicant has filed no information disclosure statements since filing the notice of appeal.

For these reasons, withdrawal of the finality of the office action is requested.

II. RESPONSE TO EXAMINER'S REJECTIONS SET FORTH IN THE OFFICE ACTION MAILED AUGUST 4, 2003

In the new final office action the examiner has presented essentially the same rejections as set forth in the original final office action, yet has added the Kendall reference stating that "Kendall et al. teaches that the capacitor structure can be formed in a discrete semiconductor device or in a monolithic integrated circuit."

Applicants do not disagree with this contention, but, nonetheless, the Kendall reference does not remedy any of the deficiencies in the earlier combination based on Saia et al. in view of Watanabe. Recall, as carefully explained in the appeal brief of record, the combination of Saia and Watanabe is a piecemeal reconstruction that is inconsistent with the cited art.

First, as noted at pages 6 and 7 of the appeal brief, it is improper to reconstruct the capacitor plate 52 of Saia as though it were an interconnect conductor. Secondly, the only semiconductor regions that Saia or Watanabe disclose or imply are regions of integrated circuitry such as the source/drain region of a FET (which the examiner has noted from the Watanabe reference). But, in this regard, Saia clearly teaches away from the examiner's contention. That is, see Figure 7 and Col. 4, lines 54 – 60 of Saia which specifically teaches connecting the electrical conductor 20 to a chip pad 77 instead of a semiconductor region in the circuit chip 68.

By all appearances, the examiner only relies on the fact that it is well known that that when capacitor structures are formed in integrated circuits they are connected to semiconductor layers. This is not applicants' invention and nothing in the Kendall reference calls for a piecemeal and inconsistent reconstruction of the art of record.

Again, as noted in the appeal brief, applicants have readily acknowledged that the circuit chip 68 may be a monolithic integrated circuit. However, it is clear that the "stack" of Saia is **not** part of the circuit chip 68 or part of any monolithic integrated circuit. Thus Saia's teaching to connect the conductor 20 to the pad 77 in order to make electrical contact with circuit chip 68 is inconsistent with the examiner's speculative and piece meal reconstruction. Clearly it would be improper to substitute a semiconductor layer for a metal contact or other pad such as the pad 77.

It is only the applicants that teach forming the claimed stack "between first and second levels of conductor" and connecting these same conductors to a semiconductor layer with the first and third conductive layers commonly connected. Nothing in the Kendall reference can correct the deficiencies and inconsistencies present in this piecemeal reconstruction.

Applicants' invention addresses the need to advance the level of semiconductor process integration by increasing the capacitance on a monolithic semiconductor integrated circuit without increasing the area consumed over a semiconductor region. There is no teaching or suggestion in any of the references to reconstruct the Saia reference, i.e., to make Saia's module into any monolithic integrated circuit; or by changing Saia's capacitor plate 52 into an interconnect conductor (e.g., a runner) for connection to a semiconductor layer.

III. CONCLUSIONS

In summary, it is improper to combine the references because they teach away from the invention and the combination is fraught with technical incompatibilities.

For all of these reasons it is submitted that the claims are in condition for allowance and the application should be passed to issuance. If the examiner refuses to allow the application, it is at least incumbent upon the examiner to withdraw the finality of the office action and to respond to the substantive deficiencies presented above. In fact, these same substantive deficiencies were fully presented in the appeal brief and no response has been provided by the examiner.

Allowance is therefore requested.

Respectfully submitted,

Ferdinand M. Romano

Ferdinand M. Romano
Attorney for Applicant(s), Reg. No. 32752

Date: 3 November 2003